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STATE-OF-THE-ART ION-IMPLANTED LOW-NOISE GaAs MESFET AND MONOLITHIC AMPLIFIER

K.G. Wang and S.K. Wang

Hughes Aircraft Company
Torrance Research Center
3100 West Lomita Boulevard, Torrance, CA 90509

ABSTRACT

State-of-the-art GaAs low-noise MESFET and monolithic amplifier have been fabricated using a high yield, planar, ion-implantation process. A 0.5μm-gate FET has achieved 1.2 dB noise figure with 8.8 dB associated gain at 12 GHz and 1.7 dB noise figure with 6.6 dB associated gain at 18 GHz. A two-stage monolithic amplifier using this FET process has achieved 1.8 dB noise figure with 23.6 dB associated gain at 9.5 GHz. The dc yield of the amplifier chips is better than 40 percent.

INTRODUCTION

Ion implantation is the preferred technology for high volume, low cost production of GaAs monolithic circuits.[1,2] However the best reported GaAs low-noise MESFETs used either epitaxial materials or ion-implantation into buffer layers.[3,4,5,6] This paper reports the state-of-the-art GaAs low-noise FETs fabricated using a direct ion implantation process. A two-stage X-band monolithic amplifier using this FET process has also demonstrated state-of-the-art performance comparable to the results by Lehmann and Heston.[7]

FABRICATION OF LOW-NOISE FETs

The key factors to achieving high performance low-noise FETs are minimizing parasitic resistances and maintaining high transconductance near pinch-off.[8,9] Low energy implants generally produce steep doping profiles which will result in high FET transconductance near pinch-off. However, this advantage is usually offset by the high source resistance associated with the shallow channel layer.[10]

In this work, we are able to maximize the FET transconductance near pinch-off by using a 70 Kev Si implant to form a heavily doped, abrupt channel layer, and at the same time minimize the source resistance by using selective implants to form N^+ layers under the source and drain contacts. The cross-section of the device structure is illustrated in Figure 1.

The devices reported here use Hughes' standard 0.5 x 300μm low-noise PI-300 FET geometry.[10] The process starts with the channel layer formation by direct implantation of $^{28}Si^+$ ions into an LEC semi-insulating GaAs substrate, with 70 Kev energy and 7×10^{12} cm^{-2} dose. Next, N^+ contact layers are selectively implanted into the source/drain region to minimize the source resistance. The implanted wafers are subsequently capless-annealed at 850°C for 30 minutes under As_4 overpressure. The doping profile of the channel layer is shown in Figure 2. The peak carrier concentration is about 5×10^{17} cm^{-3} with an effective channel thickness of about 1200 Å. This process produces FETs with an average saturation current of 160 mA/300μm and a standard deviation of 3.6 percent across a two inch wafer.

The FET ohmic contacts are formed using standard AuGe/Ni/Au metallization and thermal alloying. The 0.5μm gate is defined by contact photo-lithography and lift-off process. Next, a Ti-Au overlay metal is formed for low resistance bonding. Fabrication is completed by a

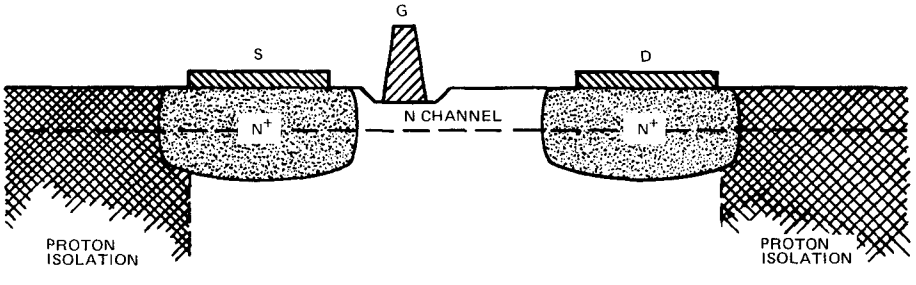

Figure 1. Cross-section of the ion-implanted GaAs low-noise MESFET.

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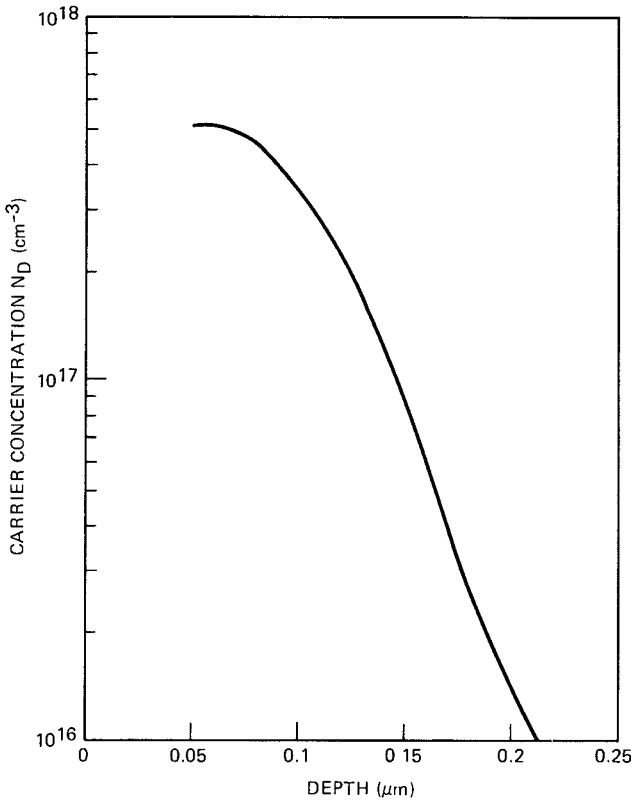

Figure 2. The measured carrier concentration profile from a 70 Kev and $7x10^{12}cm^{-2}$ Si^+ direct ion implantation into a GaAs LEC semi-insulating substrate.

precision lapping and backside metallization. After scribe and break, each device is dc tested and wire-bonded in a 50Ω line fixture for RF testing.

LOW NOISE FET PERFORMANCE

Figure 3 shows a typical I-V characteristic of the low-noise FET. The Idss is in the 40 to 46 mA range with a 1.2 to 1.4 V pinch-off voltage. The typical transconductance is 160 ms/mm near Idss and 100 ms/mm near pinch-off. The flat current saturation in Figure 3 indicates a low output conductance. The dc yield of the FET chips is 47 percent.

RF testing at 12 and 18 GHz has been conducted on the 0.5μm-gate low-noise FETs. At 12 GHz, the average noise figure is 1.4 dB with 9.0 dB associated gain, while the best device measures 1.2 dB noise figure with 8.8 dB associated gain and 14.2 dB maximum available gain as shown in Figure 4. At 18 GHz, the same device shows a 1.7 dB noise figure with 6.6 dB associated gain. Note in Figure 4 that the minimum noise figure is measured at a very low channel current indicating that the device maintains a high quality channel characteristics (high transconductance, etc.) near the channel-substrate interface. These results represent the best low-noise performance from a 0.5μm-gate ion-implanted GaAs MESFET.

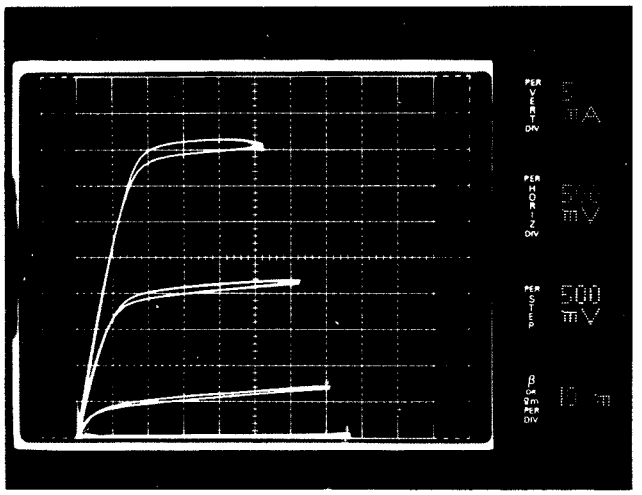

Figure 3. Typical I-V characteristics of a ion-implanted 0.5 μm-gate low-noise GaAs FET (Wg = 300 μm), showing high transconductance near pinch-off and low output conductance.

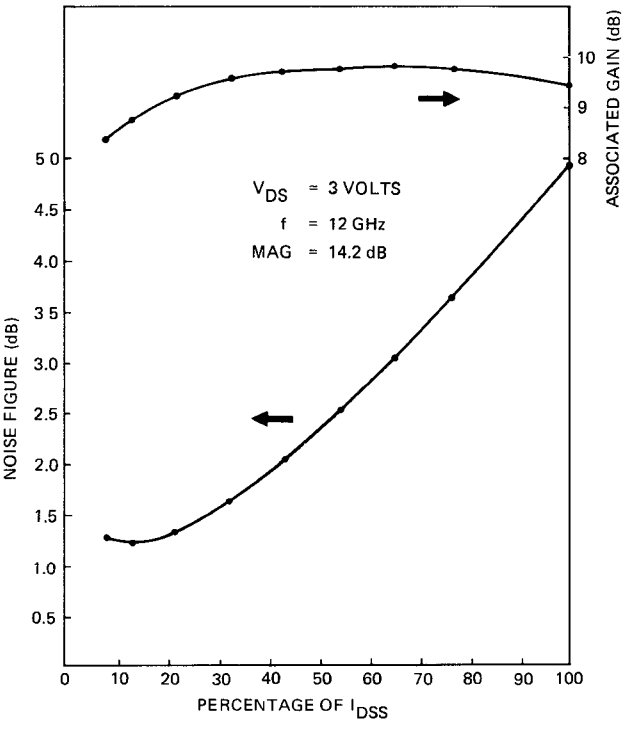

Figure 4. Noise performance of a 0.5 μm gate FET at 12 GHz.

MONOLITHIC LOW NOISE AMPLIFIER PERFORMANCE

The main objective of this work is to develop a high performance, production-adaptable FET process for MMIC applications. As a test vehicle, an X-band two-stage low-noise monolithic amplifier[2] has been fabricated using this new FET process. The dc yield of the amplifier chips is 42 percent. The noise figure and associated gain of the amplifier from 8 to 9.5 GHz are plotted in Figure 5. The gain roll-off beyond 9 GHz is the result of non-optimized matching circuits. Nonetheless, the 1.8 dB noise figure and 23.6 dB associated gain at 9.5 GHz match the best performance from an X-band monolithic low-noise amplifier.[7] Optimized matching circuits based on the new FET model would promise to further improve the amplifier performance.

CONCLUSION

A state-of-the-art GaAs low-noise MESFET has been developed using a production-adaptable ion implantation process. 1.2 dB noise figure with 8.8 dB associated gain has been achieved at 12 GHz and 1.7 dB noise figure with 6.6 dB associated gain has been obtained at 18 GHz. This excellent device performance is attributed to the high doping density in a shallow channel layer, coupled with selective N^+ implants in the source/drain region. A non-optimized monolithic amplifier using this FET process has demonstrated 1.8 dB noise figure with 23.6 dB associated gain at 9.5 GHz. The dc yields for the FET and amplifier chips are 47 percent and 42 percent respectively. These results clearly demonstrate that with proper design and process, direct ion implantation is capable of producing low cost and high performance low-noise MESFETs and MMICs.

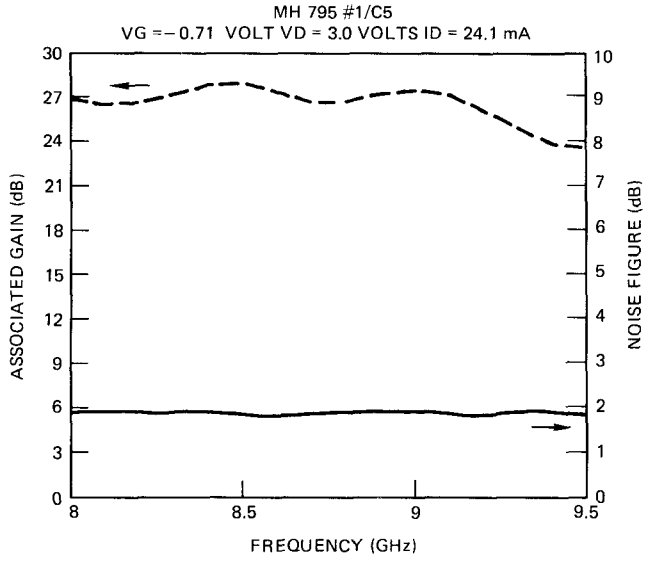

Figure 5. Noise figure and associated gain versus frequency from a two-stage monolithic amplifier.

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